九齊科技股份有限公司

Nyquest Technology Co., Ltd.

DATA SHEET

NY6B Series

Single-Chip 4-bit MCU with 16 I/O & 6-ch Speech/Midi

Version 1.1

May 31, 2017

Revision History

Version	Date	Description	Modified Page
1.0	2016/11/25	Formally release.	-
1.1	2017/05/31	1. Add description that a 0.1uF power capacitor nearby PB_VDD is necessary if LDO regulator is enabled. 2. Modify DC Characteristic. 3. Modify application circuit.	12 16 17

1. 概述

NY6B 系列產品為多功能單晶片CMOS語音合成4位元微控制器，提供6通道的語音/MIDI合成功能，所有的通道或部分的通道可同時播放語音或MIDI。語音和MIDI音色的合成方式都可採用高保真度的 4-bit, 5-bit 混合式 ADPCM 演算法或 10-bit PCM，最高採樣率可達44.1KHz，可提供接近CD的音質。NY6B 是特別設計用來做MIDI合成應用，除了提供256階ADSR包絡(Attack-Decay-Sustain-Release envelope)作為音色合成，還加上精準的+/-0.5%內阻震盪與內建的硬體自動調音功能。因此，NY6B 能準確地合成MIDI音符，讓音效逼近真實樂器。

NY6B 內建了九齊科技最新開發的250KHz超採樣雜訊過濾演算法(Noise Filter with 250KHz Over-Sampling)，能夠有效的消除雜訊並大幅改善語音和音樂的品質，具有16階數位音量控制可以讓使用者依需求調整合成語音或音樂的音量效果。有提供兩種音訊輸出方式供選擇，12-bit DAC 輸出與12-bit PWM 輸出。因此，NY6B 語音/音樂品質是所有方案中最好的選擇。

NY6B 內建硬體SPI 介面(Mode0/Mode3) 給Channel-0 使用，能自動讀取外部 SPI 記憶體的資料來播放語音(Auto Mode, 24-bit 定址)，也能手動送指令/定址讀取外部 SPI 記憶體的資料(User Mode)；另外，針對類比訊號偵測內建了一個電壓比較器，還提供一組可經由軟體控制的低壓復位計數線路以便使用者做電壓管理。

NY6B 的RISC精簡指令集架構可以很容易地做編輯和控制，共有75條指令，大多數指令都是1個時序即能完成，可以讓使用者輕鬆地以程式控制完成不同的應用。除了一般操作模式之外，NY6B 也提供待機模式(Halt mode)與慢速模式(Slow mode)，以節省功耗。

2. 功能

- 寬廣的工作電壓： 2.0V ~ 5.5V。
- 4-bit RISC 精簡指令集架構的微控制器，共有75條指令。
- 共有11個母體，最大母體的ROM容量為208Kx10-bit，程式和資料共用同一塊ROM。

產品編號	語音長度 (秒) @6kHz	ROM 容量 (10-bit)
NY6B005A	5.0	16k x 10
NY6B008A	8.3	24k x 10
NY6B011A	11.7	32k x 10
NY6B018A	18.3	48k x 10
NY6B025A	25.0	64k x 10
NY6B035A	35.0	88k x 10
NY6B045A	45.0	112k x 10
NY6B055A	55.0	136k x 10
NY6B065A	65.0	160k x 10
NY6B075A	75.0	184k x 10
NY6B085A	85.0	208k x 10

- 336x4-bit RAM，分成6頁，每頁56x4-bit。

- 2MHz 指令頻率。
- 提供慢速模式(Slow mode)，可降低功耗。(+/- 3.0% 精準度)
- 提供待機模式(Halt mode)，可節省功耗，靜態電流(Isb)小於1uA。
- 內建精準的 +/- 0.5% 內阻震盪。
- 提供低壓復位(LVR=1.9V)，看門狗計時(WDT)，I/O復位功能(External Reset)。
- 特殊的LVR硬體計數器，可經由軟體來做低電壓管理。
- 一組8-bit 計時計數器可針對不同的應用提供多種時脈。
- 一個中斷輸入可連結到一組獨立的堆棧(Stack)，並有多種中斷來源可以使用。
- 一組低壓偵測 (LVD) 可用來監控當前電壓狀態，避免電壓不穩定導致系統出錯。
- 一組LDO 穩壓器可供電給 SPI Flash。
- 硬體 SPI 介面可連接外部 SPI 裝置做資料讀取，支援雙電源供電，例如 NY6B @ 5V, SPI @ 3V。
- 16根彈性的雙向I/O腳，每個I/O腳都有單獨的暫存器控制為輸入或輸出腳。
- 每個雙向I/O腳都可分別設定不同的輸入和輸出選項。針對輸入腳的三種選項：有上拉電阻的輸入腳、無上拉電阻的輸入腳、或是有暫存器控制上拉電阻的輸入腳。針對輸出腳的三種選項：有一般輸出電流 (Normal Drive Current, Normal Sink Current)、大電流的輸出腳(Large Sink Current)、或是定電流輸出(Constant Sink Current)。 *(光罩選擇)*
- 共用I/O腳可以當作外部復位輸入、紅外線載波輸出、比較器、SPI 介面。 *(光罩選擇)*

External reset (Reset)	PA3/Reset
IR carrier (IR)	PA2/IR
Comparator	PA1/VIN
	PA0/VIP
SPI	PB0/CSb
	PB1/SCK
	PB2/SDO *(MOSI)*
	PB3/SDI *(MISO)*

- 紅外線載波頻率可供選擇，同時載波之極性也可以根據數據作選擇。
- 內建電壓比較器，可用來偵測類比訊號。比較器的輸出結果可以用來執行中斷和喚醒，也可做為計時計數器的來源。
- 最多可6通道同時播放，每個通道皆可任意地被指定為語音或MIDI通道。

- 提供 4-bit / 5-bit 混合式 ADPCM, 10-bit PCM 高音質的語音/MIDI音色合成演算法，256階ADSR包絡用於MIDI合成編輯。
- 新型專利的250KHz超採樣雜訊過濾演算法，在不增加ROM容量的前提下，可大幅加強訊噪比並提供優質聲音。
- 內建16階數位音量控制，可用於語音/音樂合成。
- 內建自動調音硬體 (Automatic Tone-Calibration)，可自動對每個音色頻率做零誤差的精準校準。
- 一組 12-bit DAC 純硬體輸出，可以外加放大線路來驅動喇叭；一組 12-bit PWM 硬體輸出，可以直接驅動喇叭或蜂鳴片。
- 提供超大音量PWM (Ultra PWM) 輸出，可以直接輸出更大音量，輸出語音不需外加三級管放大。

1. GENERAL DESCRIPTION

The NY6B series IC is a powerful 4-bit micro-controller based sound processor. There are 6 channels that are configured as speech or MIDI, and all of these 6 channels or part of them can be played with speech or MIDI simultaneously. By using the high fidelity 4-bit, 5-bit mixed ADPCM or 10-bit PCM speech/ MIDI timbre synthesis algorithm with up to 44.1KHz sample rate, NY6B produces high quality voices. As NY6B is specially designed for MIDI synthesis application, it provides Attack-Decay-Sustain-Release method (ADSR) with 256-level envelope for Patch (instrument) synthesis. NY6B can precisely synthesize any tone frequency of MIDI with +/- 0.5% accurate internal oscillation and automatic Tone-Calibration. Therefore NY6B melody quality is very close to real instrument.

Moreover, NY6B is equipped with new Nyquest's developed high-quality noise filtering algorithm of 250KHz over-sampling, which can remove noise in order to improve speech and melody quality greatly. Up to 16-level digital volume can be applied to final synthetic speech or melody that is tailored for applications of volume adjustment. NY6B provides two kinds of audio outputs with fine resolution, one is 12-bit current-type D/A converter (DAC) and the other is 12-bit Pulse-Width-Modulation (PWM). Therefore NY6B speech/ melody quality is the best choice among all solutions.

Hardware SPI (Mode0/Mode3) is supported for Channel-0 voice data automatically (auto mode, 24-bit addressing capability) and user data (user mode) fetch from external SPI memory. Voltage comparator is built-in for analog signal detecting applications. Software low voltage reset counting mechanism is provided for low power management.

The RISC MCU architecture is very easy to program and control, various applications can be easily implemented. There are 75 instructions, and most of them are executed in single cycle. Besides normal operation mode, NY6B also provides Halt mode (or Sleep mode) and Slow mode to minimize power dissipation.

2. FEATURES

- Wide operating voltage range: 2.0V to 5.5V.
- 4-bit RISC type micro-controller with 75 instructions.
- There are 11 bodies. 208Kx10-bit ROM is the maximum. Program and voice data share the same ROM space.

Product	Voice Duration (sec) @6kHz	ROM Size (10-bit)
NY6B005A	5.0	16k x 10
NY6B008A	8.3	24k x 10
NY6B011A	11.7	32k x 10
NY6B018A	18.3	48k x 10
NY6B025A	25.0	64k x 10
NY6B035A	35.0	88k x 10
NY6B045A	45.0	112k x 10
NY6B055A	55.0	136k x 10
NY6B065A	65.0	160k x 10
NY6B075A	75.0	184k x 10
NY6B085A	85.0	208k x 10

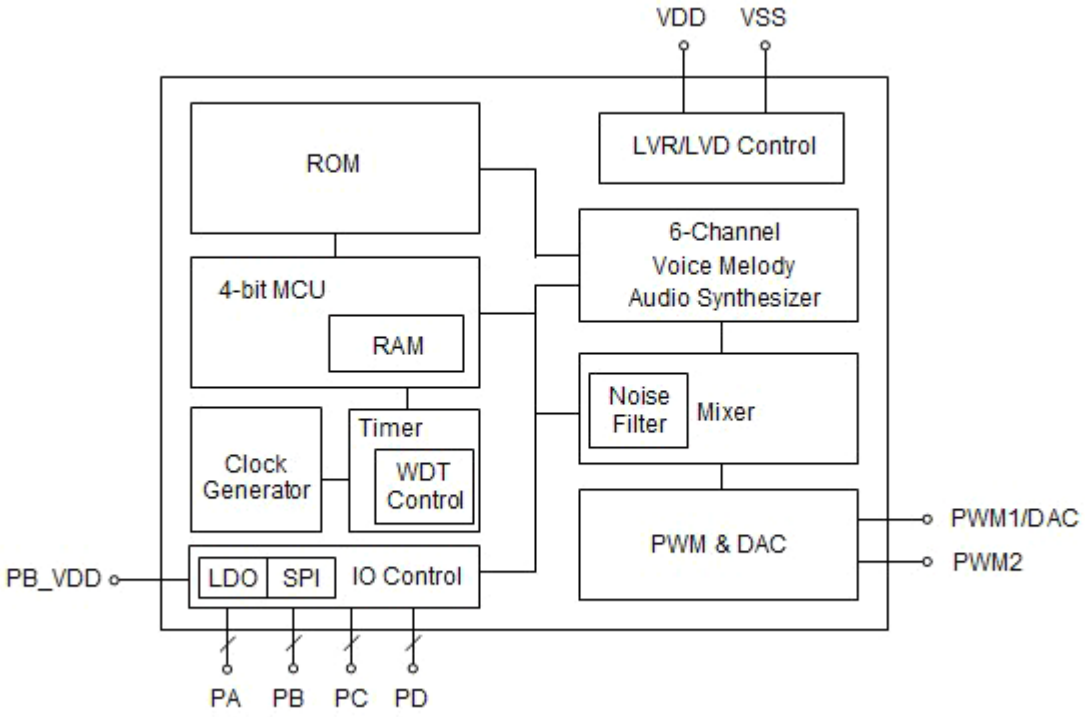
- 336x4-bit RAM, divided into 6 pages.
- 2MHz instruction frequency.
- Slow mode to operate with low power consumption (+/- 3.0% accuracy).
- HALT mode to save power, less than 1uA@3V standby current.
- Built-in RC oscillation is accurate with +/- 0.5% frequency deviation.
- Low voltage reset (LVR=1.9V), watch-dog reset and I/O port reset are all supported to protect the system.
- Special hardware for LVR occurrence counting by program to manage low battery system operation.
- One interrupt entrance with an independent stack, multiple interrupt sources.
- 8-bit timer counter is applied to multiple clock source for various application.
- Low Voltage Detector (LVD) is built-in for monitoring the status of power and protect malfunction if unstable power is given.
- LDO regulator is supported for the power supply of SPI flash.
- Hardware SPI for external SPI devices data access. Dual power system operation supported (ex: NY6B @ 5V, SPI @ 3V).
- 16 flexible Bi-direction I/Os. Direction of each I/O is independently controlled by individual register bit.

- Each Bi-direction I/O pin can be optioned as different input and output function. For the input option, users can select one of three kinds of option: input with pull-high resistor, input without pull-high resistor, or input with register-controlled pull-high resistor (high-to-low wakeup only). For the output option, users can select one of three kinds of option: output with normal drive/sink sink current, large sink current or constant sink current. *(Mask option)*
- Shared pins to provide IR carrier, comparator, SPI interface and external reset feature. *(Mask option)*

External reset (Reset)	PA3/Reset
IR carrier (IR)	PA2/IR
Comparator	PA1/VIN
	PA0/VIP
SPI	PB0/CSb
	PB1/SCK
	PB2/SDO *(MOSI)*
	PB3/SDI *(MISO)*

- Infrared output: optional IR carrier frequency and optional data high/low IR output supported.
- Built-in voltage comparator for analog signal detection applications. Comparator output flag can be configured to generate interrupt and wakeup. Also, the flag can be used for timer counter clock source for specific application.
- Maximum of 6 channels can be played simultaneously, and each channel can be arbitrarily assigned as speech or MIDI channel.
- New high fidelity 4-bit / 5-bit mixed ADPCM or 10-bit PCM speech synthesis algorithm and ADSR with 256-step envelope for MIDI synthesis.
- Patented noise filtering algorithm with 250KHz over sampling to enhance signal-to-noise ratio and provide excellent sound quality without ROM size increase.
- 16-level digital volume control for synthetic speech/melody.
- Built-in hardware automatic Tone-Calibration of near-zero frequency deviation for precise tone frequency.
- High quality 12-bit D/A converter or 12-bit PWM driver.
- PWM driver can be normal PWM or Ultra PWM.

3. BLOCK DIAGRAM



4. PAD DESCRIPTION

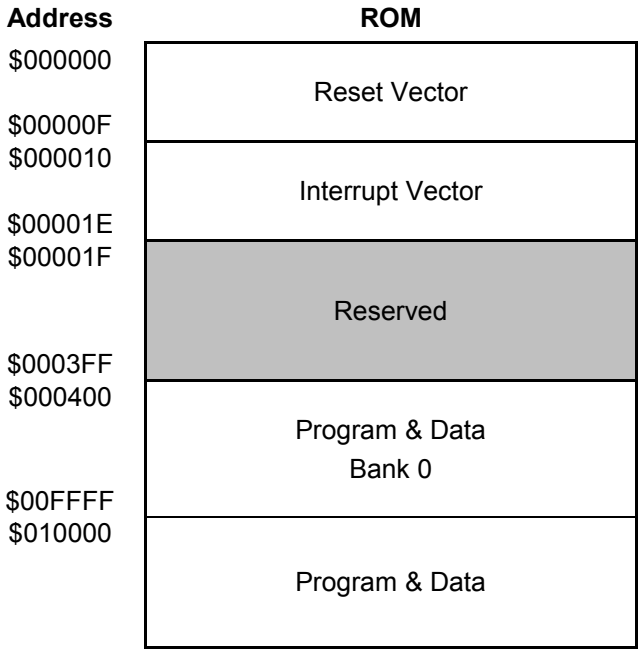
Pad Name	ATTR.	Description
VDD1~2	Power	Positive power.
GND1~3	Power	Negative power.
PA0/VIP	I/O	Bit 0 for Port A, or positive input of comparator.
PA1/VIN	I/O	Bit 1 for Port A, or negative input of comparator.
PA2/IR	I/O	Bit 2 for Port A, or IR carrier output.
PA3/Reset	I/O	Bit 3 for Port A, or external reset input.
PB_VDD	Power	Power for Port B and external component.
PB0/CSb	I/O	Bit 0 for Port B, or chip select pin for SPI interface.
PB1/SCK	I/O	Bit 1 for Port B, or serial clock pin for SPI interface.
PB2/SDO	I/O	Bit 2 for Port B, or serial data output pin (MOSI) for SPI interface.
PB3/SDI	I/O	Bit 3 for Port B, or serial data input pin (MISO) for SPI interface.
PC0~3	I/O	Bit 0~3 for Port C.
PD0~3	I/O	Bit 0~3 for Port D.
PWM1/DAC	O	PWM1 output or DAC output.
PWM2	O	PWM2 output.

5. MEMORY ORGANIZATION

There are maximum 208K words ROM, 6x56 nibbles of RAM and 32 nibbles of dedicated System Register.

5.1 ROM

A large program/data/voice single ROM is provided, and its structure is shown below. The reserved region contains system information and can't be utilized by users. After reset process is completed, NY6B will start program execution from address 0x000. Because program page size is 64K words defined by 16-bit length address of ROM, allowable range of unconditional branch instructions JMP and CALL are limited by program page size. However, combining with 3-bit BANK register, the total program size is 512K words. If users want to branch to program which is located beyond current program bank, user can change the BANK register first and then execute JMP or CALL instruction.



5.2 RAM

There are 6 pages of RAM, each page of RAM contains 56 nibbles. It's total 336 nibbles. The page of RAM defined by MPG (PAGE0~5), and its initial is PAGE0. Memory Registers of RPT0~5 and ROD1~2 will occupy address space from 0x00 to 0x07. Moreover, this address space of PAGE0~5 are mapped to the same dedicated registers. As consequence, the address space of PAGE0~5 RAM which can be used by programmer is 0x08~0x3F.

In addition to the immediate addressing mode, the indexed addressing mode is also supported. The page and address of the indexed RAM should be stored into {PAGE, RPT1[1:0], RPT0} or {PAGE, RPT3[1:0], RPT2} first, and users can read from or write in the XMD0/XMD1 memory register to realize the indexed RAM access.

6. CLOCK GENERATOR

The system clock is 2MHz, which is fast enough for many kinds of applications. The clock generator is a Ring oscillator, and users can only select the internal resistor oscillation (INT-R). The INT-R oscillator accuracy is up to ± 0.5%.

7. TIME BASE INTERRUPT

There are four kinds of time base interrupt period provided by NY6B: 0.256ms, 0.512ms, 1.024ms and 16.384ms. Users can select them by writing register INT[3:0].

If polling method is adopted to know time base status, reading BTF[3:0] register can get the status of these four timer base. If interrupt method is adopted to implement a tick timer for application, writing 1 to register INT0[3:0] will enable corresponding time base interrupt.

8. IO PORTS

There are at most 16 I/O pins, designated as PAx through PDx, and x=0~3. All the I/O pins are bi-directional. An individual and independent register bit can determine the direction of each I/O pin.

Using as input pin of each I/O, there are 3 kinds of mask option. Users can select input with pull-high resistor, input without pull-high resistor, or input with register-controlled pull-high resistor (high-to-low wakeup only).

If users want to enable/disable pull-high resistor by register during program execution, only high-to-low level change on this pin can wakeup NY6B. On the other hand, if the pull-high resistor is fixed by option, either high-to-low or low-to-high level change on this pin can wakeup NY6B.

The pull-high resistor of all the I/O pins has two kinds of option: weak and strong. The weak one is about 1MΩ@3V for normal application and the strong one is about 100KΩ@3V usually for key matrix function. When users decide this option, the same strength of pull-high resistor will be applied to every I/O pin.

Using as output pin of each I/O, there are 3 kinds of mask option. Users can select output with normal drive current and normal sink current, normal drive current and large sink current, or normal drive current and constant sink current.

The I/O pin PA2/IR is also a multi-function pin. PA2 can be optioned as IR carrier pin and IR carrier frequency can be determined by a 5-bit option. There is another option to determine IR carrier how is present according to data value is high or low.

The I/O pin PA3/Reset can be used as external reset pin by setting option. When PA3 is used as external reset, an active low signal on this pin will reset NY6B.

9. SPI CONTROL INTERFACE

Port PB is assigned for SPI interface, PB0 to CSb, PB1 to SCK, PB2 to MOSI and PB3 to MISO. For the connection with external Flash, the applied pins are MOSI, MISO and SCK. The MISO is the input pin to receive data from the external device, and the MOSI is the output pin to deliver data. The SCK is the output pin to offer the clock signal, and configured as Option (8M/4M/2M/1M Hz). However, the CSb of enable pin for the external device can share with one of IO ports and define it as output.

SPI interface is built-in to communicate with external flash through Port PB. In order to keep the same voltage level as external devices, PB_VDD is designated for Port PB power, and it can be also the power for external SPI devices. There are two typical applications for PB_VDD connections. Case 1: PB_VDD is connected to VDD when PB_VDD status is set as floating. Case 2: PB_VDD is connected to external SPI VDD pin when PB_VDD status is set as internal LDO regulator (3.3V).

As the mentioned, the internal LDO regulator, it powers external flash and Port PB 10mA @3V. Users have to enable internal LDO by $SPIV before transmitting data or else the power for SPI interface will be abnormal. Unless power is supplied by another source, external VDD, or the communication with SPI flash will be failed.

There are two modes designed in NY6B to communicate with SPI flash. User Mode is to access serial flash based on common SPI 8-bit protocol. NY6B acts as Master side to write command or address and read back data through serial flash. Auto mode is built-in protocol to communicate with SPI flash automatically. It supports users to access SPI flash and perform voice data to channel 0. Users just follow the specific start-up procedure, NY6B will automatically playback the voice data stored in flash and maximum of SPI size supported is up to 128M bits.

10. COMPARATOR

A voltage comparator is built-in for analog signal detection applications. Users can apply PA0 / PA1 to inputs of comparator by mask option. Basically, the output of comparator is represented for the level difference between VIP (PA0) and VIN (PA1). If output of comparator goes high, VIP is with higher level than VIN; low, VIP with smaller level than VIN. The comparator flag will be set to high while the level of VIP is bigger than VIN and won't be kept high even if the flag is clean and VIP is still bigger than VIN. Because the flag is controlled by a positive-edge clock source of register, the level of VIP has to be lower than VIP and the flag is clean by writing 0 to $INTF1. The flag will be launched while the level of VIP is bigger than VIN again.

11. LDO REGULATOR

A LDO regulator is built-in as the power of PB0~3 to support SPI applications. Users can set 3.3V and internal power from LDO regulator through register $SPIV for SPI interface. The LDO regulator supplies enough power consumption for reading data from SPI flash, but programming SPI flash won't be supported due to less supply current of LDO (10mA). Particularly, the LDO regulator is designated for SPI interface, not normal IO. If users apply to control high-consumption device, i.e. LED, the application won't work as expected. Please note that a 0.1uF capacitor nearby PB_VDD pin is necessary to stabilize the voltage if LDO regulator is enabled.

12. LOW VOLTAGE DETECTOR (LVD)

There is one hardware voltage detector in NY6B. It offers four levels for various application, 2.4V, 2.7V, 3.6V and 4.1V controlled by register $LVD. The voltage detection function has to be enabled first, then select specific level for application, the flag will go to high while VDD is higher than selected level. User can check power status by setting different level and monitoring the flag. In general, for 2-battery application, 2.4V/2.7V will be chosen; 3-battery application, 3.6V/4.1V.

13. AUDIO SYNTHESIZER

NY6B provide 6-CH Speech/MIDI synthesizer to play voice and patch-wave melody. All synthesis is provided by hardware and each channel can synthesize voice/MIDI independently.

For each synthetic channel, it has one 8-bit envelope register to multiply with voice data or patch-wave data. There is a hardware Mixer to add these 6 synthetic data to provide final result. However, before the first PLAY instruction is executed, users have to wait about 40us after Mixer is enabled.

The final result can be controller by a 4-bit register to adjust its volume and then it is sent to Audio Output to produce analog audio signal to drive external speaker.

NY6B provide two kinds of Audio Output: one is 12-bit DAC and the other is 12-bit PWM direct-drive.

13.1 Voice

NY6B supports 10-bit PCM and encoded 4-bit / 5-bit mixed ADPCM speech data. The PCM voice quality is higher, but it occupies double ROM space than the ADPCM one. By cooperating with embedded noise filter of 250KHz over-sampling, it could decode high fidelity voice data even if you adopt ADPCM voice. It means you could store longer voice duration or provide more kinds of patch at lower sampling rate but enrich user's applications without degradation of sound quality.

13.2 Midi

NY6B provide three kinds of method to construct a patch-wave of timbre (instrument). The first method is to record a complete waveform, then play it by playing whole wave only. It is usually called "Head Only". This is the best way to represent a best quality melody at the expense of ROM space.

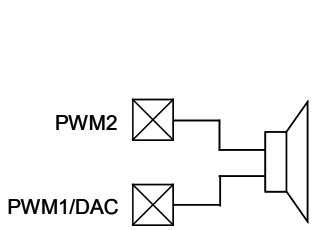
The second method is called "Head wave + Tail Loop" with envelope information representing ADSR (Attack-Decay-Sustain-Release). It is the recommended way to construct a patch-wave in NY6, which can provide high quality melody without sacrificing too much ROM space.

The third method is to use periodic portion of an instrument to represent a patch. It is called "Tail Loop". This method will occupy less ROM space with acceptable audio quality.

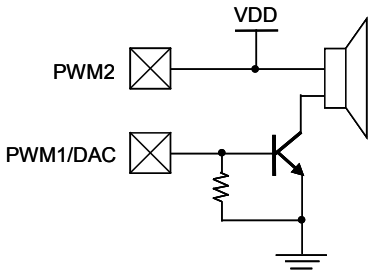
13.3 Audio Output

NY6B provide two kinds of audio output: one is 12-bit DAC and the other is 12-bit PWM direct-drive. By programming register CHARC[3] with appropriate value, users can select one of them to synthesize audio signal to drive external speaker.

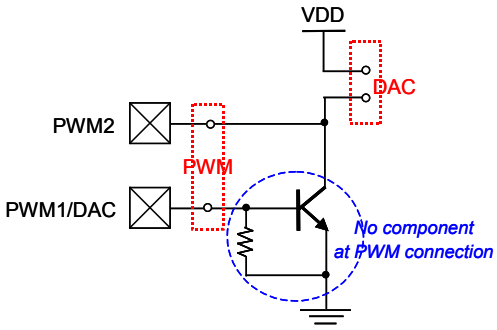
Moreover NY6B provides a pad detecting mechanism. The pad detecting mechanism detects the PWM2 pad during the reset initialization period, and sets the initial value of register CHARC[3] as PWM if the PWM2 connection is floating, or sets the initial value of register CHARC[3] as DAC if the PWM2 connection is high. In conclusion, connect the speaker to PWM1 and PWM2 only if using PWM, otherwise connect PWM2 to VDD if using DAC. Since the mechanism sets only the initial value of CHARC[3], don't change the value of register CHARC[3] if the pad detecting mechanism is adopted.



PWM Output Connection



DAC Output Connection



PWM/DAC Connection Together

When using the PWM output, we provide an option of normal PWM current or ultra PWM current for different customer demand. The ultra PWM consumes more current and makes sound louder.

13.4 Envelope Control

During speech synthesis or melody synthesis, there is one 8-bit envelope register (ENVH and ENVL), which can store the envelope information. Therefore NY6B can provide 256 levels envelope control and users can use it as alternative of volume control.

13.5 Volume Control

There are 16 steps volume control, which can be applied to synthetic digital data for the Mixer output no matter DAC or PWM direct-drive is selected.

When users write value to register VOL[3:0], this value will multiply with Mixer output to adjust the volume of final synthetic result.

14. WATCH-DOG TIMER (WDT)

To recover from program malfunction, the NY6B IC supports an embedded watch-dog timer reset. Users have to clear the WDT periodically to prevent from timing up with a reset generation.

Typically, the minimum time-up period of the WDT is about 28ms and users can clear WDT through instruction CWDT.

15. OPERATING MODE

NY6B provide 3 kinds of operating mode: Normal, Slow and Halt mode. After power is turned on, NY6B will start its reset process. The power on stable time is about 131ms. After reset process is completed, NY6B will enter Normal mode.

In Normal mode, the system clock is 2MHz. User can implement sorts of application in this mode. On the other hand, users can select Slow mode or Halt mode to save power consumption.

15.1 Slow Mode

NY6B will enter Slow mode if SLOW instruction is executed. The system clock of Slow mode is about 14.3 times slower than that of Normal mode, and the frequency accuracy is +/- 3.0%. The instruction will not be executed at Slow mode.

NY6B can wake up from Slow mode by interrupt request or level change on I/O pin. The stable time after wake up from Slow mode is about 50us.

15.2 Halt Mode

NY6B will enter Halt mode if the HALT instruction is executed. At Halt mode, system clock is completely disabled and all IC functions stop to minimize the power consumption.

The only way to wake up NY6B from Halt mode is level change on I/O pin. The stable time after wake up from Halt mode is about 50us.

16. ELECTRICAL CHARACTERISTICS

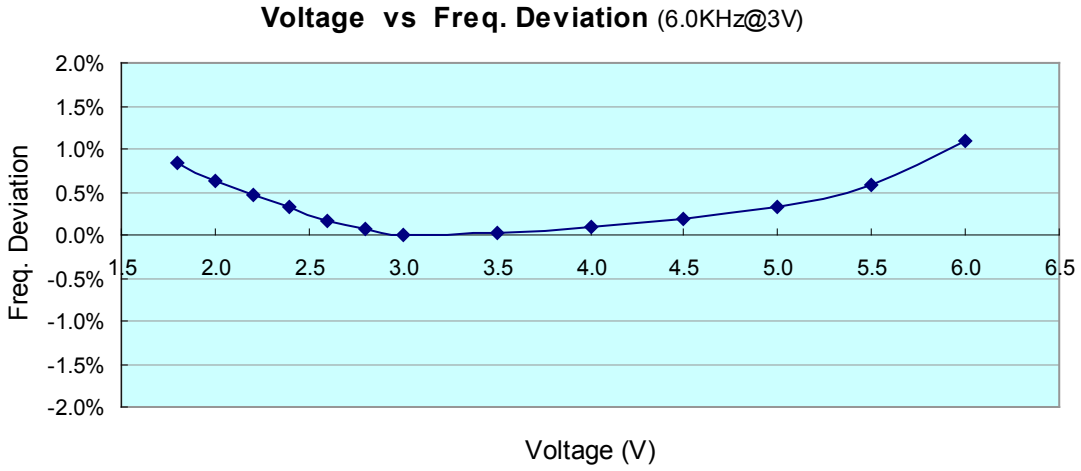
16.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
Vdd - Vss	Supply voltage	-0.5 ~ +6.0	V
Vin	Input voltage	Vss–0.3V ~ Vdd+0.3	V
Top	Operating Temperature	0 ~ +70	°C
Tst	Storage Temperature	-25 ~ +85	°C

16.2 DC Characteristics

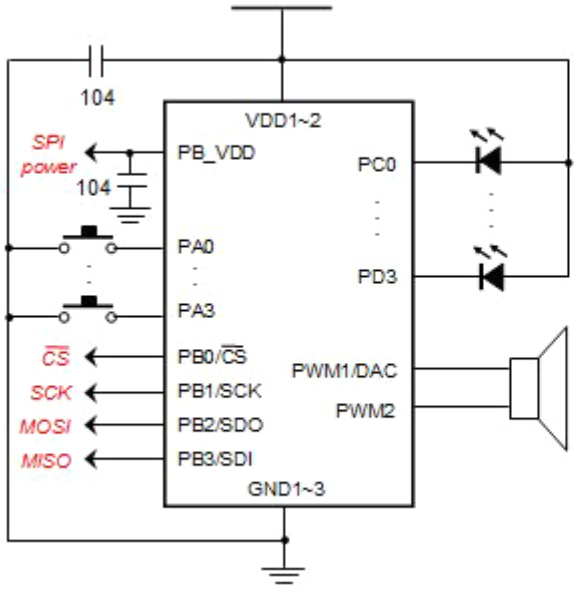
Symbol	Parameter		VDD	Min.	Typ.	Max.	Unit	Condition
VDD	Operating voltage			2.0	3	5.5	V	2MHz
I_{SB}	Supply current	Halt mode	3		0.1	0.5	uA	Sleep, no load
			4.5		0.1	0.5		
I_{SL}		Slow mode	3		50		uA	BT=16.384ms, no load
			4.5		60			
Iop		Operating mode	3		1.4		mA	2MHz, no load
			4.5		2.6			
I_{IL}	Input current (Internal pull-high)	Weak (1M ohms)	3		2.5		uA	V_{IL}=0V
			4.5		7.4			
		Strong (100k ohms)	3		30		uA	
			4.5		75			
I_{OH}	Output high current		3		-7		mA	V_{OH}=2.0V
			4.5		-11			V_{OH}=3.5V
I_{OL}	Output low current (Normal current)		3		10		mA	V_{OL}=1.0V
			4.5		16			
	Output low current (Large current)		3		20		mA	
			4.5		30			
	Output low current (Constant current)		3		18		mA	
			4.5		21			
I_{PWM}	PWM output current (Normal)		3		60		mA	Load=8 ohms
			4.5		100			
	PWM output current (Ultra)		3		80		mA	
			4.5		125			
I_{DAC}	DAC output current		3		1.4		mA	Half scale
			4.5		1.6			
△F/F	Frequency deviation by voltage drop		3		-0.5		%	$\frac{Fosc(3.0v)-Fosc(2.4v)}{Fosc(3v)}$
			4.5		0.5			$\frac{Fosc(4.5v)-Fosc(3.0v)}{Fosc(4.5v)}$
△F/F	Frequency lot deviation		3	-0.5		0.5	%	$\frac{Fmax(3.0v)-Fmin(3.0v)}{Fmax(3.0v)}$
Fosc	Oscillation Frequency		-	1.90	2	2.05	MHz	VDD=2.0~5.5V

16.3 Voltage vs. Frequency

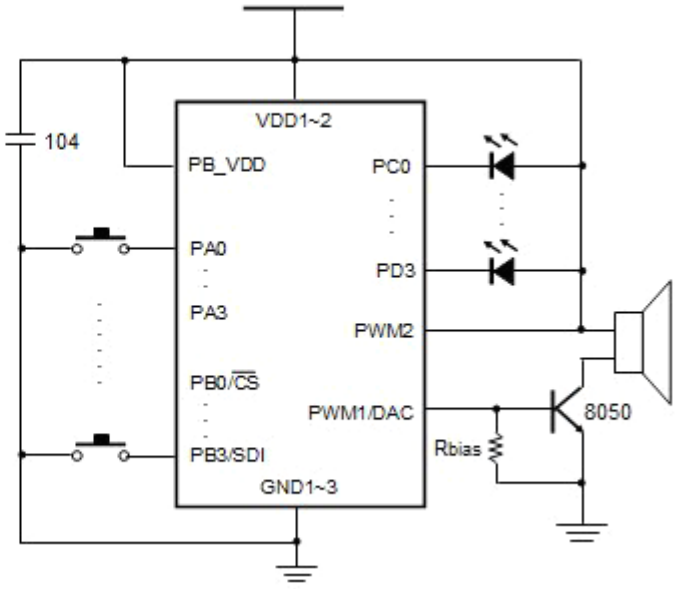


17. APPLICATION

(1) PWM Direct-Drive *(PB_VDD is set as LDO=3.3V)*



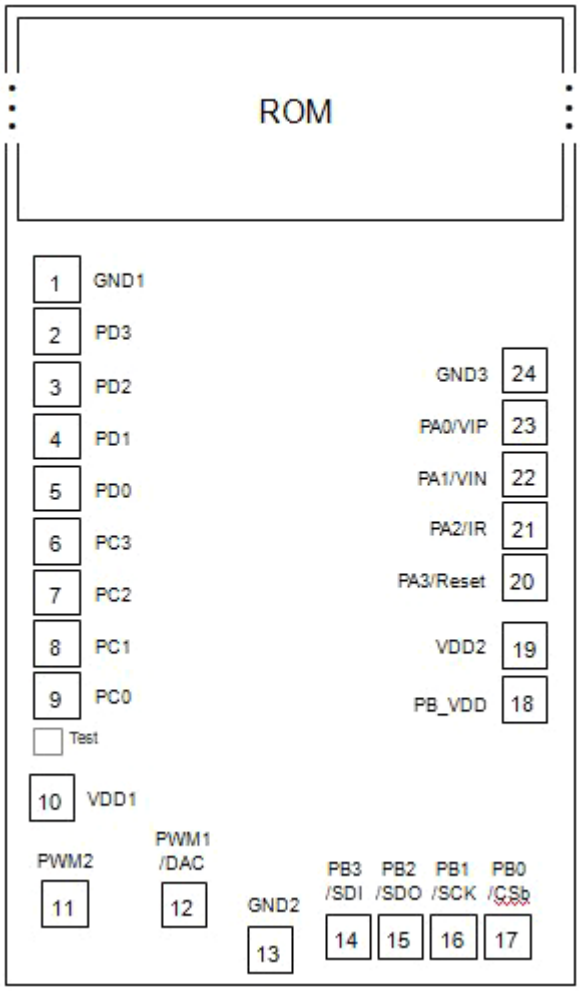
(2) DAC Output *(PB_VDD is set as floating)*



Note 1: If PB_VDD is set as LDO internally, PB_VDD pad is an output for the power of external SPI devices. And a 0.1uF capacitor is necessary to stabilize the LDO output voltage.

Note 2: If PB_VDD is set as floating internally, PB_VDD pad must be connected to VDD or external power supply.

18. DIE PAD DIAGRAM



* The IC substrate must be connected to GND or Floating.